semiconductor chip 21 and the wiring substrate 25 repeat expansion and contraction by heat generated by operations (on/off operation) of the device. However, the coefficient of thermal expansion of the semiconductor chip 21 is about 3.5 ppm whereas the coefficient of thermal expansion of the wiring substrate 25 is about 16 ppm in case of a printed board and about 8 ppm in case of an alumina substrate. Due to this difference in the coefficient of thermal expansion between the semiconductor chip 21 and the wiring substrate 25, the solder balls 26 are alternately subject to compressive stress and tensile stress. As a result, the solder balls 26 are broken at an early stage due to thermal fatigue, which causes electric disconnection, resulting in a signal transmission stop or a power supply stop.--

Cancel C1

IN THE CLAIMS:

Amend claim 1 as follows:

C2 --1. (amended) A mounting structure of a semiconductor device comprising:

a semiconductor chip which is provided with a plurality of solder balls arranged in a grid array;

a wiring substrate which is provided with a plurality of connection pads; and

an insulating sheet which has a plurality of leads and which is provided between said semiconductor chip and said wiring substrate,